

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Li Attorney Docket: 2004 P 50201 US
Filed: Herewith Examiner: TBD
Serial No.: TBD Art Unit: TBD
For: Transistor with Shallow Germanium Implantation Region in Channel

Mail Stop: Patent Application
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

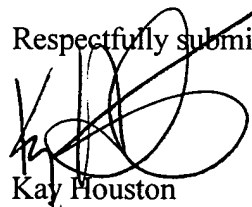
The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08a & 08b that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed concurrently with the patent application.

March 22, 2004

Date

Respectfully submitted,



Kay Houston
Attorney for Applicant
Reg. No. 38,495

Slater & Matsil, L.L.P.
17950 Preston Rd., Suite 1000
Dallas, TX 75252
(972) 732-1001 (phone)
(972) 732-9218 (fax)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>			Complete if Known		
			Application Number	TBD	
			Filing Date	HEREWITH	
			First Named Inventor	Li	
			Art Unit	TBD	
			Examiner Name	TBD	
Sheet	1	of	2	Attorney Docket Number	2004 P 50201 US

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
	1	US-6,621,131 B2	09-16-2003	Murthy, et al.	
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	TBD
				Filing Date	HEREWITH
				First Named Inventor	Li
				Art Unit	TBD
				Examiner Name	TBD
Sheet	2	of	2	Attorney Docket Number	2004 P 50201 US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	2	KING, A.C., <i>et al.</i> , "Surface Proximity Effect on End-of-Range Damage of Low Energy Ge ⁺ Implantation," Ultra Shallow Junctions 2003, Seventh International Workshop on: Fabrication, Characterization, and Modeling of Ultra-Shallow Doping Profiles in Semiconductors, April 27–May 1, 2003, pp. 447–450, Santa Cruz, CA, USA.	
	3	STRAUBE, U.N., <i>et al.</i> , "Adverse Effect of Ge ⁺ Implantation for Fabrication of SiGe PMOS," Electronics Letters, December 6, 2001, pp. 1549–1550, Vol. 37, No. 25.	
	4	SELVAKUMAR, C.R., <i>et al.</i> , "SiGe-Channel n-MOSFET by Germanium Implantation," IEEE Electron Device Letters, August, 1991, pp. 444–446, Vol. 12, No. 8, IEEE, New York, NY, USA.	
	5	JIANG, H., <i>et al.</i> , "Electrical Properties of GeSi Surface- and Buried- Channel p-MOSFET's Fabricated by Ge Implantation," IEEE Transactions on Electron Devices, January, 1996, pp. 97–103, Vol. 43, No. 1, IEEE, New York, NY, USA.	
	6	JOHN, S., <i>et al.</i> , "Strained Si n-Channel Metal-Oxide-Semiconductor Transistor on Relaxed Si _{1-x} Ge _x Formed by Ion Implantation of Ge," Applied Physics Letters, April 5, 1999, pp. 2076–2078, Vol. 74, No. 14, American Institute of Physics, College Park, MD, USA.	
	7	LIU, K.C., <i>et al.</i> , "A Deep Submicron Si _{1-x} Ge _x /Si Vertical PMOSFET Fabricated by Ge Ion Implantation," IEEE Electron Device Letters, January, 1998, pp. 13–15, Vol. 19, No. 1, IEEE, New York, NY, USA.	
	8	NGUYEN, N.V., <i>et al.</i> , "Characterization of the Interface Between Ge ⁺ -Implanted Crystalline Silicon and its Thermally Grown Oxide by Spectroscopic Ellipsometry," Journal of Applied Physics, January 15, 1990, pp. 599–603, Vol. 67, No. 2, American Institute of Physics, College Park, MD, USA.	
	9	HÖCK, G., <i>et al.</i> , "High Hole Mobility in Si _{0.17} Ge _{0.83} Channel Metal-Oxide-Semiconductor Field-Effect Transistors Grown by Plasma-Enhanced Chemical Vapor Deposition," Applied Physics Letters, June 26, 2000, pp. 3920–3922, Vol. 76, No. 26, American Institute of Physics, College Park, MD, USA.	
	10	SHANG, H., <i>et al.</i> , "High Mobility p-Channel Germanium MOSFETs with a Thin Ge Oxynitride Gate Dielectric," 2002, 0-7803-7463-X/02, IEEE, New York, NY, USA.	
	11	LEE, M.L., <i>et al.</i> , "Strained Ge Channel p-Type Metal-Oxide-Semiconductor Field-Effect Transistors Grown on Si _{1-x} Ge _x /Si Virtual Substrates," Applied Physics Letters, November 12, 2001, pp. 3344–3346, Vol. 79, No. 20, American Institute of Physics, College Park, MD, USA.	
	12	CHUI, C.O., <i>et al.</i> , "Germanium MOS Capacitors Incorporating Ultrathin High-κ Gate Dielectric," IEEE Electron Device Letters, August, 2002, pp. 473–475, Vol. 23, No. 8, IEEE, New York, NY, USA.	
	13	CHUI, C.O., <i>et al.</i> , "A Sub-400°C Germanium MOSFET Technology with High-κ Dielectric and Metal Gate," 2002, 0-7803-7463-X/02, IEEE, New York, NY, USA.	
	14	ZOLLNER, S., <i>et al.</i> , "Optical Constants and Ellipsometric Thickness Determination of Strained Si _{1-x} Ge _x :C Layers on Si (100) and Related Heterostructures," Journal of Applied Physics, October 1, 2000, pp. 4102–4108, Vol. 88, No. 7, American Institute of Physics, College Park, MD, USA.	
	15	LEGOUES, F.K., <i>et al.</i> , "Oxidation Studies of SiGe," Journal of Applied Physics, February 15, 1989, pp. 1724–1728, Vol. 65, No. 4, American Institute of Physics, College Park, MD, USA.	
	16	PLUMMER, et al., Silicon VLSE Technology, Fundamentals, Practice and Modeling, 2000, p. 453, Prentice Hall, Upper Saddle River, NJ.	
	17	"Front End Processes," International Technology Roadmap for Semiconductor (ITRS), 2002 Update, pp. 45–62, http://member.itrs.net/ .	
	18	"Front End Processes," International Technology Roadmap for Semiconductor (ITRS), 2003 Edition, pp. 23–25, http://member.itrs.net/ .	

Examiner Signature	Date Considered
--------------------	-----------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
 †Applicant's unique citation designation number (optional). ‡Applicant is to place a check mark here if English language Translation is attached.
 This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.